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A METHOD OF IMPROVING SHORT CHANNEL EFFECT AND GATE OXIDE RELIABILITY BY NITROGEN PLASMA TREATMENT BEFORE SPACER DEPOSITION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method for improving the short channel effect and the gate oxide reliability of CMOS devices by nitrogen plasma treatment before spacer deposition.

(2) Description of the Prior Art

Conventional methods of forming CMOS gate electrodes in or over an active device region of a semiconductor substrate are well known in the art. The active device region is typically defined by field oxide regions, which electrically isolate the active region of the substrate from the surrounding surface areas of the substrate.

Substrate conductivity in the active surface area is first established by providing n/p-well impurity implants into the active surface of the substrate. In fabricating a CMOS device, a layer of gate material such as polysilicon is formed over a layer

of thin oxide that is formed over the active device region of the substrate. The polysilicon layer is then masked and both the exposed polysilicon and the underlying thin layer of oxide are etched to define a poly-silicon gate electrode that is separated from the substrate by the thin layer of gate oxide. A self-aligned implant of for instance N-type dopant then forms lightly doped diffusion (LDD) source/drain regions in the substrate as a first phase of forming the substrate N-type source/drain regions of the CMOS device. After the formation of for instance oxide sidewall spacers on the sidewalls of the polysilicon gate and of the gate oxide, a second N-type impurity implant is performed to set the conductivity of the gate region to a desired level and to complete the N+ source/drain regions of the gate electrode.

Contact surfaces of the gate electrode may then be salicided by depositing for instance a layer of titanium over the structure, more specifically over the exposed surfaces of the N+ source/drain regions and the gate electrode. The deposited titanium is annealed, thereby causing the titanium to react with the underlying N+ silicon of the substrate of the source/drain regions and the doped polysilicon gate to form titanium salicide over these surfaces.

The gate electrode is completed by forming a layer of dielectric material, typically silicon oxide, over the gate electrode. Contact openings are etched in the dielectric and a metallization layer is formed to provide contacts to the salicided surfaces of the source/drain regions and over the polysilicon gate.

Semiconductor device performance improvements require the reduction of device dimensions from which follows in increase in device density. As devices and the therefrom created circuits are scaled down to sub-0.25 μm dimensions for Ultra Large Scale Integrated (ULSI) technology devices, the quality of the spacers that are created over sidewalls of the gate electrode becomes increasingly more important in view of the increased demands of device insulation. Continued reduction in device dimensions imposes increased demands on the profile of the impurity implants, which results in the need to reduce the thermal cycle of the gate electrode.

During conventional processing steps for the creation of a gate electrode, specifically during the etch of the layer of gate material to create the gate electrode, the etch results in damage to the silicon substrate, which is exposed during the etch, and to sidewalls of the patterned and etched layer of gate material.

To repair this damage, a step of re-oxidation is typically performed, this step removes the damage that has resulted from the etch of the layer of gate material. The need however to reduce the thermal budget during the creation of a gate electrode imposes the need to remove the re-oxidation step. This removal of the re-oxidation must be compensated for since the damage in the silicon substrate and the sidewalls of the etched layer of gate material must as yet be prepared. There is a need for the highlighted compensation and repair of etch induced damage.

US 5,808,348 (Ito et al.) shows a nitrided gate oxide process.

US 6,373,113 B1 (Gardner et al.) shows a nitrogenated gate structure and method.

US 5,990,517 (Irino) discloses a process to introduce nitrogen into a gate dielectric.

US 5,872,049 (Gardner et al.), US 5,567,638 (Lin et al.) and US 5,189,504 (Nakayama et al.) are related patents.

SUMMARY OF THE INVENTION

A principal objective of the invention is to prevent etch damage during the creation of a gate electrode while maintaining a low thermal budget.

In accordance with the objectives of the invention a new method is provided for the creation of gate spacers over sidewalls of a gate electrode. A layer of gate material, such as polysilicon, is deposited, patterned and etched, defining the poly gate electrode structure. LDD and pocket impurity implants are performed, the LDD profile is created by a rapid thermal anneal. Next and of critical importance to the invention, a N_2 or O_2 or N_2 based plasma treatment is performed to eliminate defects in the exposed surface of the silicon substrate and sidewalls of the defined gate electrode that occur as a result of the etch of the layer of gate material. Then gate spacers are formed.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the cross section of a substrate, active surface regions has been defined, layers of gate oxide and gate material have been deposited.

Fig. 2 shows a cross section after an etch blocking mask has been formed over the layer of gate material.

Fig. 3 shows a cross section after the layer of gate material and the layer of gate oxide have been etched, the etch blocking mask has been removed.

Fig. 4 shows a cross section during the LDD implantation into the substrate.

Fig. 5 shows a cross section during N_2 or O_2 of H_2 plasma exposure, passivating the exposed layer of gate material and the substrate.

Fig. 6 shows a cross section of the gate electrode with a layer of hydrogen or nitride or oxide bases layer formed over the gate electrode and the substrate.

Fig. 7 shows a cross section after deposition of a layer of gate spacer material.

Fig. 8 shows a cross section after formation of the gate spacers.

Fig. 9 shows the cross section of a completed gate electrode.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention is explained in detail using Figs. 1 through 8 for this purpose. Referring first specifically to Fig. 1, there is shown the cross section of a substrate 10, a layer 12 of gate oxide has been created over substrate 10, a layer 14 of gate material has been deposited over the layer 12 of gate oxide. The active surface region of substrate 10 has been defined and is bounded by the regions 11 of Shallow Trench Isolation (STI).

Substrate 10 is a conventional, monocrystalline silicon substrate. STI regions 11 in substrate 10 can be made using a number of methods. For instance, one method is the Buried Oxide (BOX) isolation used for shallow trenches. The method involves filling the trenches with a chemical vapor deposition (CVD) silicon oxide (SiO_2) and then etched back or mechanically or chemically polished to yield a planar surface. The shallow trenches etched for the BOX process are anisotropically plasma etched into the silicon substrate and are typically between 0.5 and 0.8 micrometer (μm) deep. STI regions are typically formed

around the active device to a depth between 4,000 and 20,000 Angstrom.

Another approach in forming STI regions 11 is to deposit silicon nitride on thermally grown oxide. After deposition of the nitride, a shallow trench is etched into the substrate using a mask. A layer of oxide is then deposited into the trench so that the trench forms an area of insulate dielectric which acts to isolate the devices in a chip and thus reduce the cross talk between active devices. The excess deposited oxide must be polished off and the trench planarized to prepare for the next level of metalization. The silicon nitride is provided to the silicon to prevent polishing of the masked silicon oxide of the device.

The layer 12 of pad oxide is grown on the bare silicon after the silicon surface has been cleaned. The layer consists of an about 150 Angstrom thick layer of SiO_2 and can be thermally grown on the substrate 10. The purpose of this layer 12 is to cushion the transition of the stress between the silicon substrate 10 and the subsequently deposited layer of polyimide for the formation of the gate electrode. In general, the thicker the layer 12 of pad oxide, the less edge force is being transmitted to the silicon substrate 10. Typically, a blanket pad oxide can be

formed to a thickness of about 150 Angstrom through a thermal oxidation method at a temperature of about 900 degrees C for a time period of about 10 to 20 minutes.

Layer 14 is a layer of gate material, preferably comprising polysilicon. Polysilicon layer 14 is typically deposited using low-pressure vapor deposition (LPCVD) using, for example, silane (SiH_4). The thickness of polysilicon layer 14 is between about 1,500 and 4,000 Angstrom.

Layer 14 of polysilicon is created using a number of methods, following are illustrative examples of these methods.

A heavily doped layer 14 is created by depositing a layer of polysilicon using LPCVD processing to a thickness of between about 1,500 and 4,000 Angstrom at a temperature between about 550 and 750 degrees C. An ion implant procedure, using PH_3 at an energy between about 20 and 80 KeV and a dose between about 5E14 and 5E15 atoms/cm^3 is used to dope the polysilicon layer 14. An in-situ doped layer of polysilicon can also be used for this deposition.

A lightly doped layer 14 is created by depositing a layer of polysilicon using LPCVD processing to a thickness of between about 1,500 and 4000 Angstrom at a temperature between about 550 and 750 degrees C. An ion implant procedure, using PH_3 at an energy between about 20 and 80 KeV and a dose between about 1E14 and 5E14 atoms/cm^3 is used to dope the poly layer. An in-situ doped layer of polysilicon can also be used for this deposition.

After the layer 14 of polysilicon has been deposited, an etch mask 16, Fig. 2, preferably comprising photoresist, is created over the layer 14 of polysilicon to define the structure of the gate electrode. The photoresist mask 16 is formed using conventional methods of photolithographic exposure and development.

The layer 14 of polysilicon can be etched using SF_6 and SiO_2 as etchant gasses. Polysilicon can also be etched using RIE or a high plasma density using an etchant gas having a high selectivity to oxide of layer 12, such as a gas containing clorine (Cl) species. The polysilicon gate structure can also be created via anisotropic RIE of the layer 14 polysilicon and the layer 12 of gate oxide using Cl_2 or SF_6 as an etchant.

Specifically highlighted in the cross section of Fig. 3 are the surfaces 22, the sidewalls of the gate electrode structure 14, and surfaces 24, the exposed surface of the substrate 10. These surfaces 22 and 24 are the surfaces that are typically damaged by the etch of the layer 14, Fig. 2, of polysilicon. These are therefore the surfaces that must be treated in order to remove the there-in or there-over created damage.

In the cross section that is shown in Fig. 3, the gate 14 of polysilicon is defined. LDD implant 18, Fig. 4, is now performed, self-aligned with the gate electrode 12/14, to form the Lightly Doped Diffusion regions of impurity regions 19/20 of the source/drain of the gate electrode in substrate 10.

LDD impurity implants can be performed applying a number of different parameters. A few examples are cited following.

For an P-channel CMOS device, p-type dopant species are implanted such as BF_2, for instance at a dose of between about 1.0E13 and 5.0E13 atoms/cm^3 and at an implant energy between about 40 and 60 KeV.

For an N-channel CMOS device, n-type dopant species are implanted such as arsenic or phosphorous, for instance at a dose

of between about 1.0E13 and 1.0E14 atoms/cm^3 and at an implant energy between about 30 and 80 KeV.

Numerous variations are applied in the creation of LDD impurity regions in a substrate, dependent on device design specifics and requirements.

At this time a pocket impurity implant (not shown as a separate implant since this implant generally blends in with the LDD implant, modifying the profile of the LDD impurities 19/20) may also be performed. A pocket implant establishes a high punch-through voltage that results in a low off-state current of the gate electrode. Typical processing conditions for the pocket implant are as follows:

For NMOS: In - energy: 50 to 250 keV
- dose: 5e12 to 1e14 atoms/cm^2
For PMOS: As - energy: 50 to 250 keV
- dose: 5e12 to 1e14 atoms/cm^2.

In order to improve the efficiency of the pocket implant, the pocket implant (not shown) may be performed under an angle with substrate 10.

To profile the created LDD/pocket implants 19/20, a Rapid Thermal Anneal (RPA) is applied after the LDD/pocket implantation 18 has been performed. This process of RTA drives the dopant species and changes the dopant profile. The Rapid Thermal Anneal (RTA) can for example be performed at a temperature between about 700 and 750 degrees C for a period of not longer than about 30 seconds.

In the cross section shown in Fig. 5, the surfaces 22 and 24 have been given a rough texture that represents the damage that is caused in these surfaces as previously highlighted. The structure that is shown in the cross section of Fig. 5 is now treated to a N_2 or O_2 or H_2 plasma treatment 26. The results of which are shown in the cross section of Fig. 6, that is the damage previously caused in surfaces 22 and 24 has been repaired ("passivated" in the meaning of "cancelled").

As example of processing conditions for the N_2 or O_2 or H_2 plasma treatment 26 the following parameters can be cited. The N_2 or O_2 or H_2 plasma 26 can be created under a condition in which a flow rate of a N_2 or a O_2 or a H_2 gas is about 100 sccm, a pressure of 100 Pa, a radio frequency power of about 0.005 W/cm^2, an electrode distance of about 40 mm and a substrate temperature

of about 250 degrees C, a generated nitrogen plasma is irradiated to exposed surfaces 22 and 24 for about 10 seconds.

The above highlighted plasma treatment 26 is preferably a nitrogen based plasma treatment but is not limited there-to. Plasma treatment 26 can also comprise, as indicated above, an oxide based or a hydrogen based plasma treatment, these latter two plasma treatments have been demonstrated to also passivate damage incurred in surfaces 22 and 24, Fig. 5.

The cross section shown in Fig. 6 has been provided to demonstrate that surfaces 22 and 24 are now, after plasma treatment 26, Fig. 5, free of damage. A nitrogen or hydrogen or oxide based layer 28 has been formed over the previously damaged surfaces 22 and 24, thereby filling surface irregularities such as surface pitting and generally eliminating surfaces damage.

After the plasma treatment 26, Fig. 5, has been completed, resulting in the creation of layer 28, Fig. 6, gate spacers are now formed over the no longer damaged sidewalls of gate electrode 14. For this purpose, Fig. 7, a layer 30 of gate spacer material is deposited. For gate spacer layer 30 can be used for instance silicon nitride, silicon oxide, BSG, PSG, polysilicon, other materials preferably of a dielectric nature, CVD oxide formed

from a TEOS source and amorphous materials that inhibit the deposition of epitaxial silicon thereupon.

As an example of the deposition of a layer of gate spacer material can be cited the deposition of a layer of silicon oxide, deposited using LPCVD or PECVD procedures, at a temperature between about 300 and 800 degrees C, to a thickness between about 200 and 5,000 Angstrom.

After the layer 30 of gate spacer material has been deposited, the gate spacers over sidewalls of gate electrode 14 are formed by etching the layer 30 of gate spacer material.

Silicon oxide spacers can for instance be formed via anisotropic RIE of a deposited silicon oxide layer, using CHF_3 or CF_4-O_2-He as an etchant.

The resulting gate spacers are shown as gate spacers 32 in the cross section of Fig. 7, wherein the layer 28 of hydrogen (or oxide or nitride) based plasma protection has effectively and functionally been integrated with the gate spacers and with the substrate 10.

The gate electrode, shown in cross section in Fig. 8, is now ready for completion by creating, Fig. 9:

- source and drain impurity implants 34/35 in the substrate, self-aligned with the gate spacers 32
- salicidation 36/37 and 38 of the source/drain 34/35 surfaces and the gate electrode surface 14
- a layer 40 of dielectric, and
- openings created through layer 40 and
- filling these openings with a conductive material, for the creation of interconnect 41, to the source region, 42 to the gate electrode and 43 to the drain region of the gate electrode.

The details relating to the steps highlighted in the cross section that is shown in Fig. 8 are not germane to the invention and are therefore not further discussed.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and

modifications which fall within the scope of the appended claims and equivalents thereof.